**Using the ModelSim-Intel FPGA Simulator with Verilog Testbenches**

3 files included in "Modelsim" subfolder to control Modelsim: testbench.v, testbench.tcl, and wave.do

- **testbench.v**: The purpose of a testbench is to instantiate a Verilog module that is to be simulated, and to specify values for its inputs at various simulation times

Text

Description automatically generated with medium confidence

timescale:

1ns 🡪 Unit simulation time (so that #20 is 20ns)

1ps 🡪 Granularity of time that ModelSim evaluates the signal (evaluation precision)

- **wave.do**: Specify the signals (waves) to be shown

Graphical user interface, text, table

Description automatically generated with medium confidence

- **testbench.tcl**: Specifies ModelSim commands to run simulation

Text

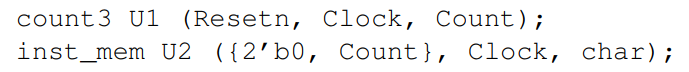
Description automatically generated

- Memory is instantiated by **inst\_mem.mif**

Text, table

Description automatically generated with medium confidence

We need to have a memory module **(inst\_mem.v)** in our code, which is connected to inst\_mem.mif



testbench.tcl compile .v files, call "vsim …" 🡪 testbench.v: Simulate signals and call our module

call "do wave.do" 🡪 Configure the waves of the signals being produced

**DESim Software**

Runs projects

Graphical user interface, application

Description automatically generated

- addern.v is the file that contains the module to be tested

- top.v is the top-level module that connects the devices (in DESim) with the module - consistent with other projects

- sim folder:

Graphical user interface, text

Description automatically generated

"Compile testbench" button in DESim will execute the **run\_compile.bat** file

Text, letter

Description automatically generated

+) Remove (if already exist) a work folder to store results of simulation

+) Compile tb.v (testbench.v) inside **tb** folder

+) Compile Addern.v and top.v

**tb.v** 🡪 Calls **top.v** 🡪 Calls **Addern.v**

"Start simulation" will execute the **run\_sim.bat** file.

Simulate project with memory module

Graphical user interface, text, application

Description automatically generated

Inside the **run\_compile** file:

Graphical user interface, text, application

Description automatically generated

- Line 1-3 copies **inst\_mem.mif** to **sim** folder

+) ModelSim requires the file to be in the sim folder to properly initialize the memory module during a simulation

+) If the file is changed in the display folder, then the latest version of the file will always be used when starting a simulation

- Line 4-6 deletes the file that sometimes causes an error to ModelSim

- You should not need to make any changes to the files in the sim or tb folder for your new project in my\_folder.

You can now open your new project in the DESim software and proceed to compile/simulate your code.

"Compile testbench" 🡪 run\_compile.bat 🡪 Copy .mif to sim & create work folder (Sets up memory)

🡪 Compiles tb.v: Setup devices (HEX0-6, LEDR0-9, VGA, etc.) Calls top module

🡪 Compiles top.v: Connect needed devices to proc module

🡪 Compiles proc.v: Our module - Calls inst\_mem module

🡪 Compiles inst\_mem.v: called by proc

"Start simulation" 🡪 run\_sim.bat